REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-20 are in the case. Claims 3, 10 and 19 have been canceled. Claims 1, 4, 5, 8, 9, 11, 12, 15, 16 and 20 have been amended. The Specification has been amended. The Title has been amended.

Regarding the rejection of Claims 3, 4, 10, 11, 19 and 20 under 35 U.S.C. § 112, first paragraph, Claims 3, 10 and 19 have been canceled, thus rendering this rejection moot. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

It is noted that the language of Claim 3 has been incorporated into independent Claim 1, the language of Claim 10 has been incorporated into independent Claim 9 and that the language of Claim 19 has been incorporated into independent Claim 16. The language so incorporated was modified in a manner that overcomes the grounds for the rejection referred to in the previous paragraph.

Regarding the rejection of Claims 1, 2, 5-9 and 12-18 under 35 U.S.C. § 102(e) as allegedly being anticipated by Kurtulik et al., Claims 1, 5, 9, 12 and 16 have been amended to overcome the rejection. As admitted in the above-mentioned Office Action, Kurtulik does not teach "a switch mode for switching between applications." This limitation has been incorporated into each of the independent claims in the case, Claims 1, 9 and 16, and thus it is respectfully submitted that Claims 1, 9 and 16 are allowable over Kurtulik. The other claims under this rejection depend, either directly or indirectly from Claim 1, 9 or 16, and so are allowable as well, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 3, 10 and 19 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kurtulik et al. in view of Rearick, Claims 3, 10 and 19 have been canceled, thus rendering this rejection moot. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

As noted above, the language of Claim 3 has been incorporated into independent Claim 1, the language of Claim 10 has been incorporated into independent Claim 9 and that the language of Claim 19 has been incorporated into independent Claim 16. The features recited in this language so incorporated is neither taught nor suggested by either Kurtulik et al. or by Rearick. As noted above, it was admitted in the above-mentioned Office action that Kurtulik does not teach "a switch mode for switching between applications." In addition, Rearick does not cure the deficiencies of Kurtulik. The recited feature of switch mode in combination with the other recited features permits an existing test scan chain to be used to provide context save and restore with minimal additional hardware. Such context save and restore can be used, for example, to allow provide multi-channel functionality with a telecommunications device comprising a single channel. In this regard, Rearick apparently relates to a method for reducing stored patterns for IC test by embedding BIST circuitry for chip logic into a scan test access port. It therefore has a different purpose than that of the claimed invention, namely, that of providing context save and restore using a scan chain. Thus, not surprisingly, it neither teaches nor suggests providing context save and restore in an integrated circuit device, the device being operable to be placed in a test mode for testing, a functional mode for executing applications, and a switch mode for switching between applications, each digital logic component operable to receive test data over a test line and a test clock signal while the device is in the test mode, to receive functional data over a functional line and a functional clock signal while the device is in the functional mode, and to receive functional data over the functional line and the functional clock signal while the device is in the switch mode. The passing reference at col. 6, II. 4-6, that the system execution clock may be used to capture normal system data into the registers comprising the scan path merely references what is stated at col. 1, II. 55-59, that scan paths may be fully integrated, i.e., that the individual registers comprising the scan path may be substituted for functional registers. It does not state or imply that the scan paths are used, *qua* scan paths, to scan

normal data, as is recited in the claims in the case. The other art of record is even less relevant.
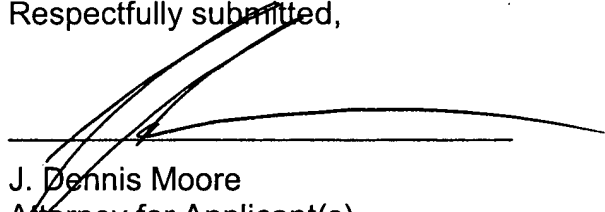
It is therefore respectfully submitted that all of the claims in the case are allowable over Kurtulik et al., Rearick, and, indeed, all of the art of record, whether considered alone or in any combination.

It is thus respectfully submitted that the claims now in the case recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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